REMARKS

This is a response to the Office Action mailed on March 24, 2005. Prior to entry of this paper, claims 1-20 were pending. Claims 1, 6-8, 10, and 16-20 are amended. Although claims 16-19 were allowed and Applicants respectfully submit that claims 6-8, and 10 were allowable prior to entry of this paper, claims 6-8, 10, and 16-19 are amended to further clarify the meaning of the claims. No change was made to the scope of claims 6-8, 10, and 16-19. Claim 21 is new. Upon entry of this amendment, claims 1-21 will be pending. No new matter is added by way of this amendment. For at least the following reasons, Applicants respectfully submit that each of the presently pending claims is in condition for allowance.

Allowed Subject Matter

The applicants appreciate the indication that claims 11-19 are allowed and thank the Examiner for his work in this matter.

Rejections under 35 USC § 112

Claim 6 is rejected under 35 USC § 112 as being indefinite for failure to illustrate the claimed features. Applicants respectfully submits that all claimed features were fully illustrated by the original language of claim 6. For example, figure 2 depicts the connection of the source of keeper transistor M8 to the source of second transistor M1 via node N2 and the drain of keeper transistor M8 to the gate of second transistor M1 via node N12. Likewise, page 3, lines 20-22 of the specification indicates, alternatively, that the drain of the keeper transistor M8 may be coupled to the source of the second transistor M1 at node N2 and the source may be coupled to the gate of the second transistor M1 at node N12. Accordingly, all features of claim 6 were properly supported by the figures and the specification. Although Applicants discuss the circuit of figure 2 in traversing this rejection of claim 6, the invention as claimed by claim 6 is not limited to this particular illustration which is discussed only by way of example. A person skilled in the art will recognize that the invention as claimed in claim 6 may be embodied in many forms without departing from the sprit and scope of the invention as claimed in claim 6.

Rejections under 35 USC § 102

Claims 1-8 are rejected under 35 USC § 102(e) as being anticipated by US Patent No. 6,693,469 to Prodanov ("Prodanov").

It is respectfully submitted claim 1 is allowable at least because Prodanov fails to disclose a second transistor that is arranged to operate "as a cascode transistor in cooperation with the first transistor as a telescopic cascode arrangement," as recited in Applicants' claim 1. A cascode transistor is typically a common gate transistor used in conjunction with a common source transistor, or other transconductance stage. *See, e.g.*, Fig. 1 of the present application, wherein M1 is a common gate cascode transistor and M0 is a common source transistor. The term cascode may refer to the combination of the common source transistor and the common-gate transistor, or may refer solely to a common gate transistor *when used in conjunction* with a common source transistor.

In figure 4 of Prodanov, neither transistor P5 nor N5 is configured as a common source transistor. Prodanov, Fig. 4; Col. 7, Lines 52-61. Accordingly, Prodanov fails to disclose the limitations of the independent claim 1. Claim 1 is thus respectfully submitted to be allowable.

As claims 2-8 depend on allowable claim 1, Applicant's respectfully request that their rejection to Prodanov be reconsidered in light of the above discussion.

Claims 1, 9-10, and 20 are rejected under 35 USC § 102(b) as being anticipated by US Patent No. 6,060,909 to Aipperspach et al. ("Aipperspach").

Aipperspach fails to disclose a keeper switch circuit including three terminals that are respectively coupled to a gate, drain, and a source of the second transistor as claimed by claim 1. The Office Action points to transistors 116 and 124 of Aipperspach, figure 1, as showing the claimed elements. However, "keeper" transistor 116 fails to have three terminals connected to the "second" transistor 124. Rather, the source of transistor 116 is connected to Vdd, not transistor 124. Accordingly, transistor 116 does not have three terminals connected to transistor 124 as Applicants claims recites.

Furthermore, in light of the discussion above, transistor 124 is not a cascode transistor because it fails to be biased as a common-gate transistor. As Aipperspach fails to disclose the limitations of the claim, Applicants respectfully submit that claim 1 is allowable.

As claims 9-10 depend on allowable claim 1, Applicants respectfully request that their rejection to Aipperspach be reconsidered in light of the above discussion.

With respect to the rejection of independent claim 20, Aipperspach fails to disclose means for coupling a source of the transistor to the gate of the transistor. Although it is unclear what the Office Action points to as the cascode transistor in rejection of claim 20, in light of the rejection of claim 1 to Aipperspach, the applicants believe that the Office Action refers to transistor 124 as the claimed cascode transistor. As above, it should be apparent that transistor 116 is not configured to couple the source of transistor 124 to the gate of transistor 124. Moreover, Aipperspach disclosed no other means for coupling the source of transistor 124 to the gate of transistor 124. Therefore, Aipperspach fails to anticipate claim 20, Applicants' respectfully submit that it is thus allowable.

New Claim 21

Applicants' respectfully submit that new claim 21 is allowable at least based upon its dependence upon claim 1. Further, for reasons similar to those discussed above, claim 21 is allowable based upon its additional recitations. Moreover, it is should be apparent to one of ordinary skill in the art that embodiments of the claimed invention may be composed from transistors of varying technologies. Such technologies may include, but are not limited to: MOS, BJT, and JFET transistors.

CONCLUSION

In light of the above amendment and remarks, applicant respectfully believes all claims are in condition for allowance and notification to that effect is requested. The Examiner is invited to contact the Applicants' representative at the below-listed telephone number if it is believed that the prosecution of this application may be assisted thereby. Although only certain arguments regarding patentability are set forth herein, there may be other arguments and reasons why the claimed invention is patentable. Applicant reserves the right to raise these arguments in the future.

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Respectfully submitted,

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